Study and Optimization of Electron Transport in sub-100nm Nanoscale Vacuum Channel Transistor

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Abstract: Recently, the nanoscale vacuum channel transistor (NVCT) has been attracting numerous attention due to its unique properties, e.g. high integration, anti-radiation capacity or fast temporal response. However, with the vacuum channel down to sub-100 nm, the physical design and electron transport mechanism of the NVCT may be different from the traditional vacuum devices. Here, the electron transport properties of the sub-100nm planar NVCT are investigated. CST STUDIO is utilized to design the structural parameters of the device, including full and aligned back gate, which proves that optimized back gate can effectively enhance the emission and transport performance.

KEYWORD: nanoscale vacuum channel transistor, electron transport performance, simulation, back gate

I. INTRODUCTION

Vacuum is an ideal medium for ballistic transport while conventional vacuum electronic devices suffer from the difficulty of miniaturization and integration. In recent years, many attempts have been made to fulfill nanoscale vacuum devices with semiconductor process. To our knowledge, Meyyappan et al. first proposed the silicon-based planar NVCTs in 2012 which performed at a low voltage (<5 V) and provided a high drive current (>3 microamperes), and explored the compatibility with semiconductor process[1-3] In 2018, Shruti Nirantar et al. demonstrated the sub-50nm NVCTs based on various types of metal, e.g. Au, W and Pt. This work verifies that NVCTs can function regularly in rough vacuum or atmospheric environment, demonstrating the superiority of nanoscale vacuum channel.[4] However, current research concentrates more on the device fabrication and compatibility with solid-state devices,[5-7] while design and optimization of electron transport performance still remains as a challenge.

In this paper, the structural parameters of sub-100nm NVCT is optimized, exploring the effects of various gate structures on the electrical properties or electron trajectories in the vacuum channel. It is observed that the electron transport performance can be effectively improved when the overlap area of gate and emitter/collector is reduced, enhancing the modulation capacity of the device.

II. METHOD

As shown in Figure 1, CST PARTICLE STUDIO is used to design and optimize the structure parameters of planar tip-to-tip NVCT. Structural parameters of the NVCT used in simulation are listed below: channel length —50nm; material of the emission/collection — aluminum cone; material of the insulation layer — 100nm-thick silicon dioxide; material of the gate — 20nm-thick aluminum. The electron trajectories and electric field distribution of the full and aligned back-gate structure are compared. We find that aligned back-gate structure can enhance the electric field intensity in the effective emission area. On the other hand, it is noted that the aligned back gate also shows strong control ability that a large emission current density can be obtained.

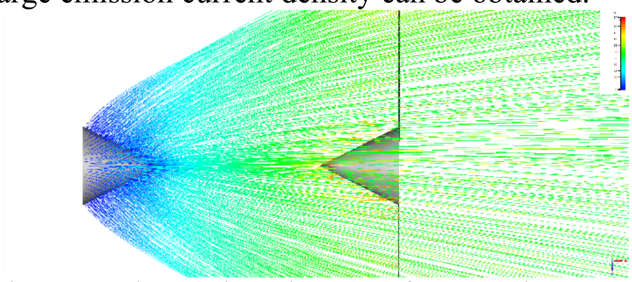

Figure 1. Electronic trajectory of nanoscale vacuum channel transistor in CST STUDIO

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