



# **Study and Optimization of Electron Transport in sub-100nm Nanoscale Vacuum Channel Transistor**

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# CONTENT



## 01 INTRODUCTION

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## 02 MAIN WORK

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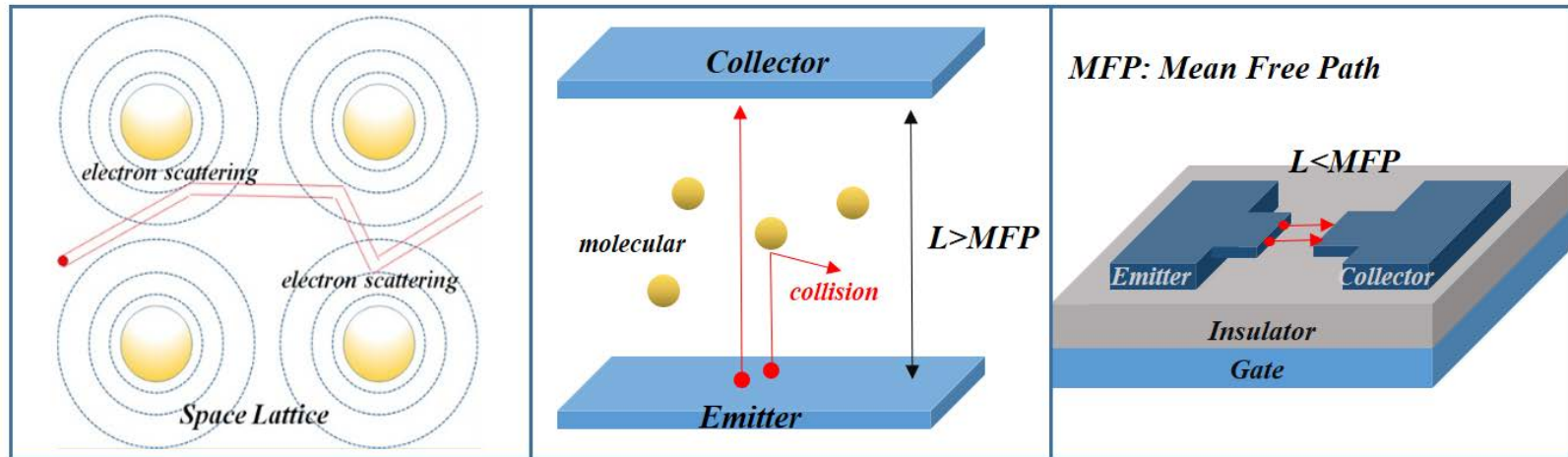
## 03 CONCLUSION

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## 04 FUTURE WORK

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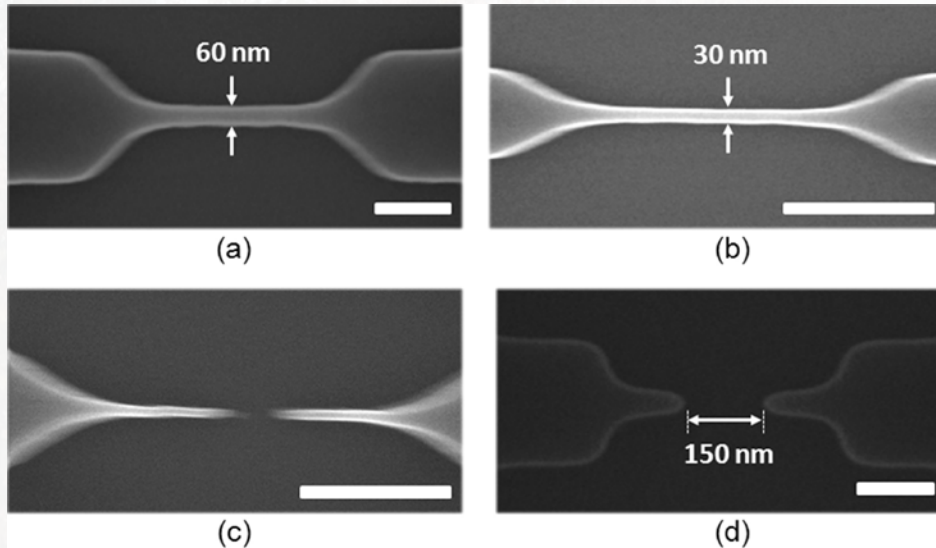


- ◆ More than Moore
- ◆ New structure and technology
- ◆ Combination of vacuum and solid-state devices
- ◆ High frequency
- ◆ Modularization and integration
- ◆ High reliability

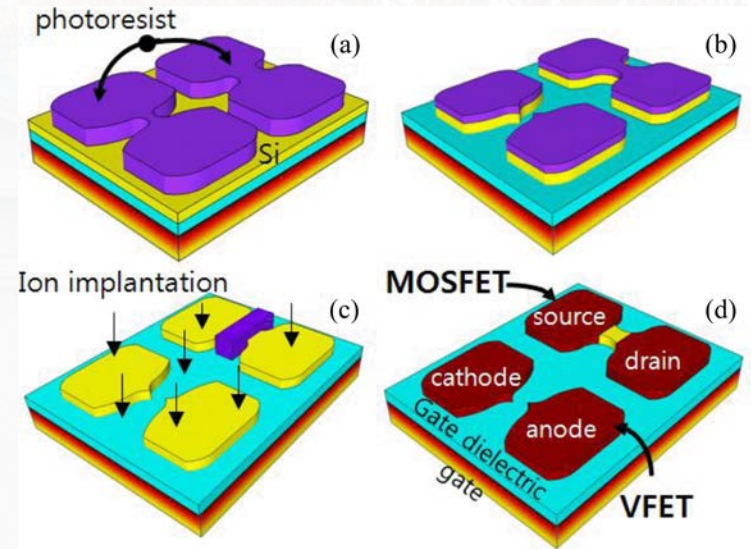




# Planner nanoscale vacuum channel transistor



Applied Physics Letters 2012, 100 (21)

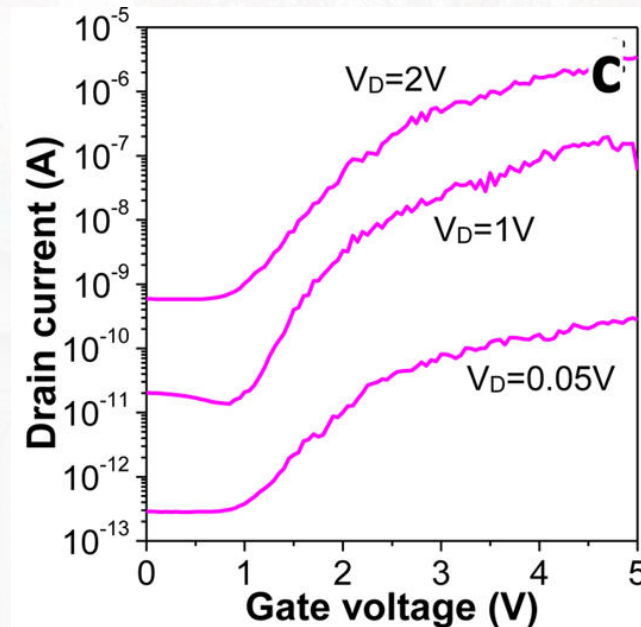
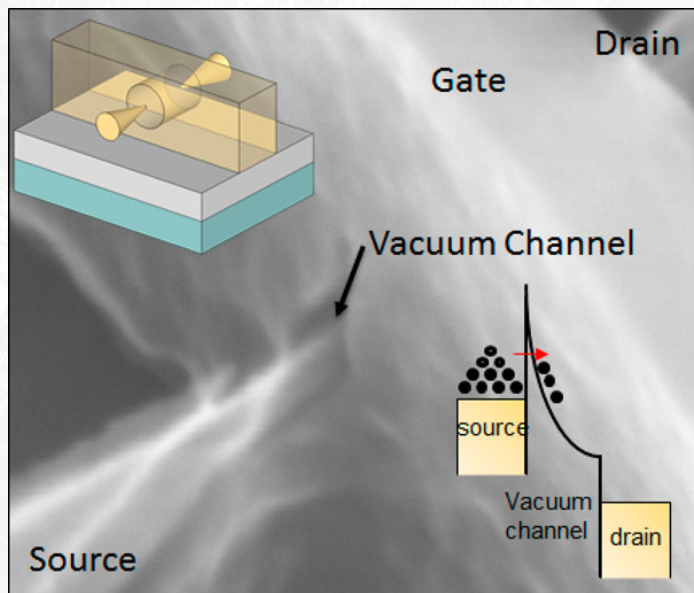


IEEE Trans on Nano 2014, 13 (3), 464-468

- ◆ Fabricated with standard silicon semiconductor process
- ◆ 150-nm-wide nanogap
- ◆ Full back gate



# Planner nanoscale vacuum channel transistor



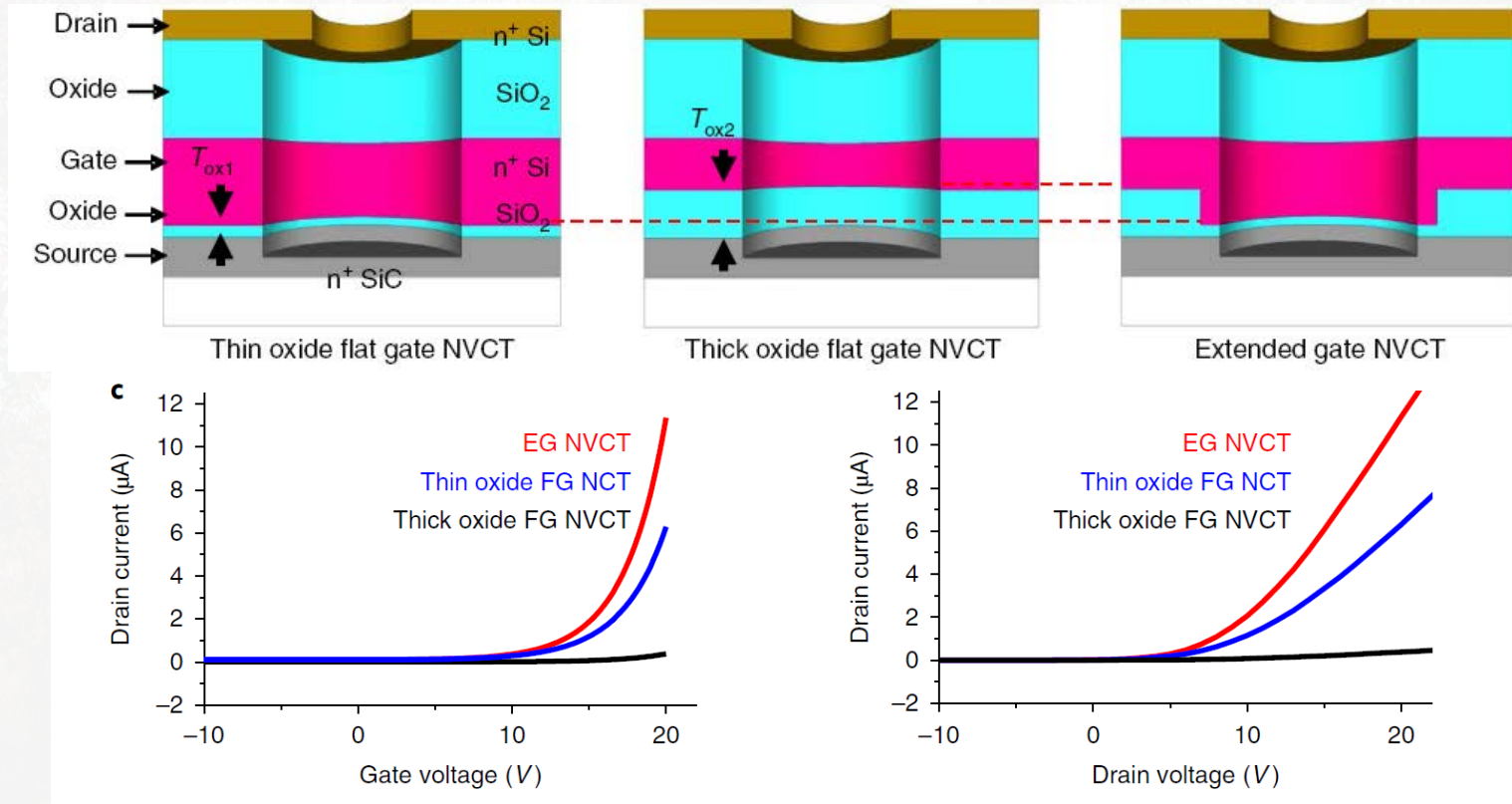
Nano Lett 2017, 17 (4), 2146-2151

- ◆ 50-nm-wide nanogap
- ◆ Threshold voltage is lower than 2v
- ◆ Surround gate enhance control ability and reliability





# Vertical nanoscale vacuum channel transistor

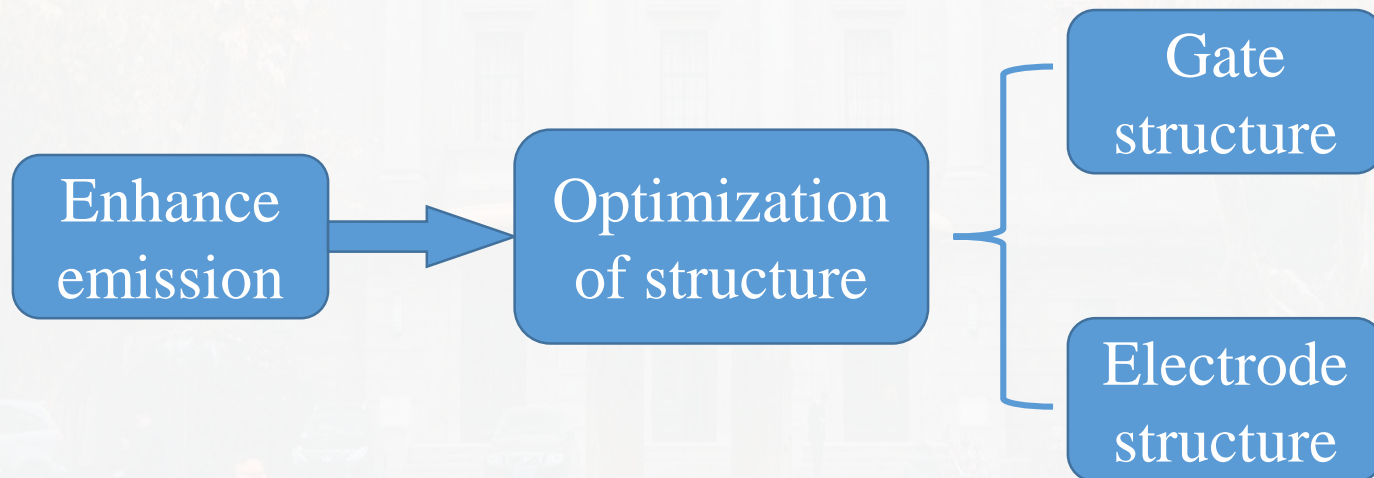


Nature Electronics 2019, 2 (9), 405-411

- ◆ Extended gate——balance between control ability and parasitic capacitance
- ◆ High reliability



- Compared to full back gate, surround gate can enhance the electric intensity and shows strong control ability.
- However, the fabrication of the planner surround gate is complicated
- The optimization of device structure is proposed





# CONTENT



**01** BACKGROUND

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**02** MAIN WORK

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**03** CONCLUSION

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**04** FUTURE WORK

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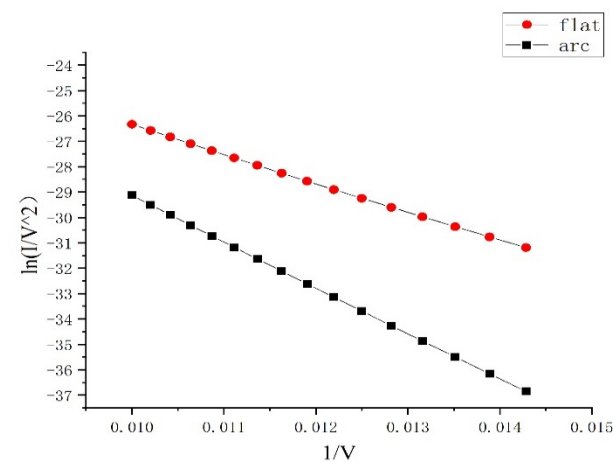
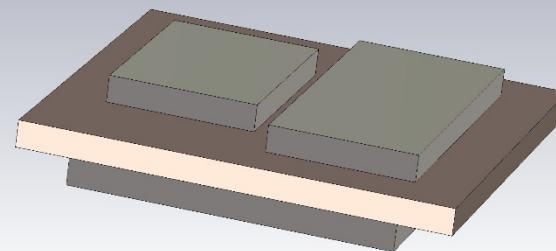
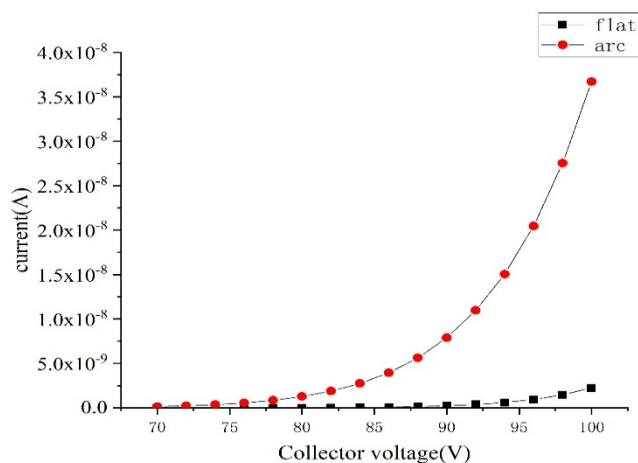
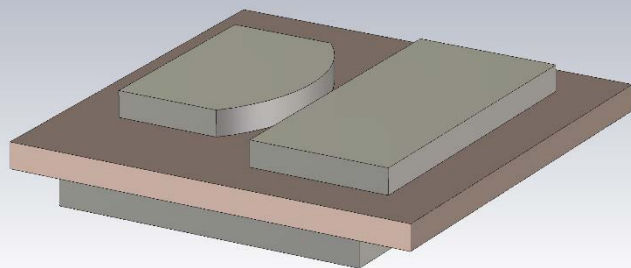




# Optimization: emitter structure



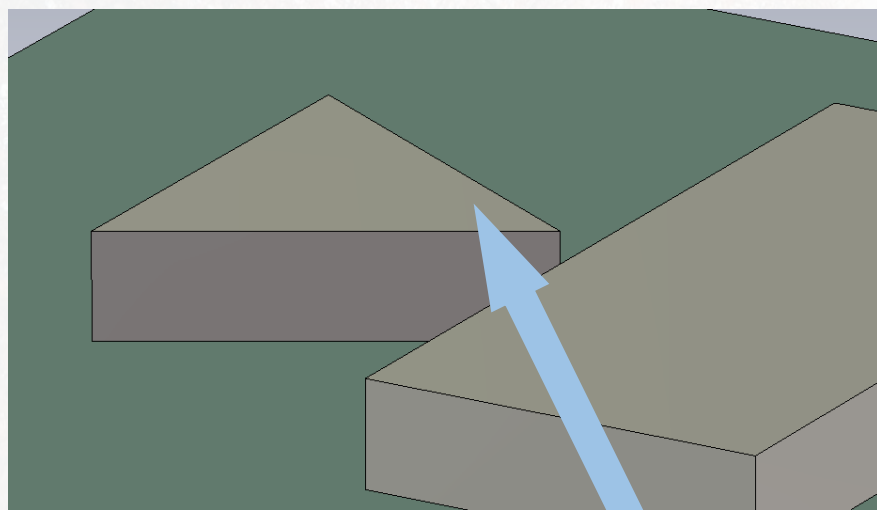
東南大學  
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	Flat	arc
Field enhancement factor	46.2	262.7
Operating current(nA)	5.2	36

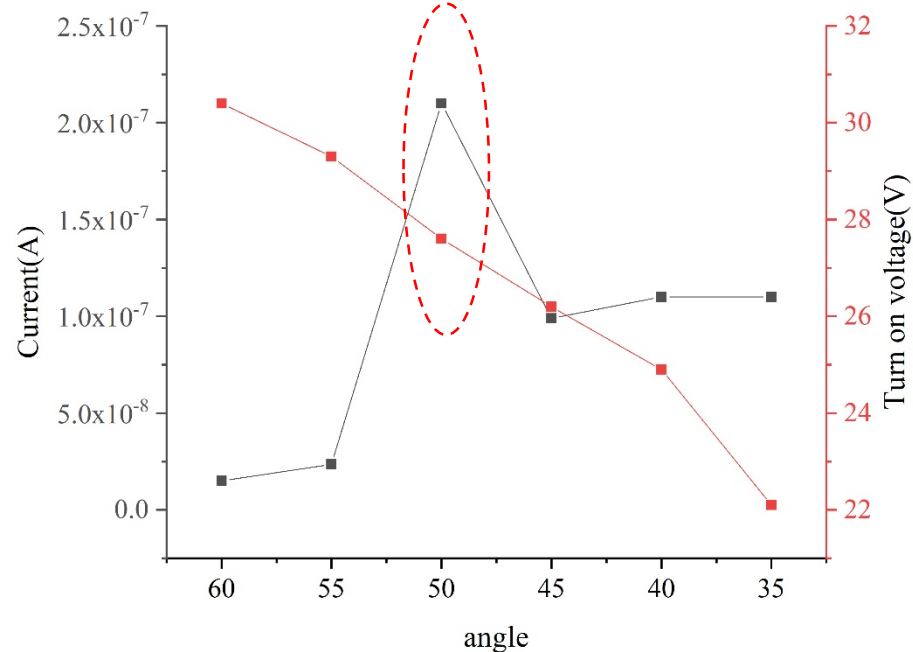


## Optimization: emitter structure



Gap width: 50nm  
Drain voltage: 30V  
Gate voltage: 15V

Top angle

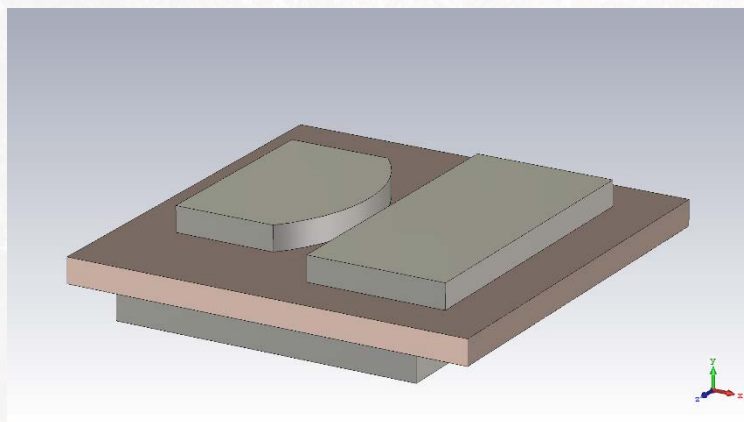


- As the angle decreases, the turn-on voltage continues to decrease as we expected
- Meanwhile, the operating current does not increase monotonously and the maximum appears at around 50°
- A balance must be achieved between the turn-on voltage and the operating current

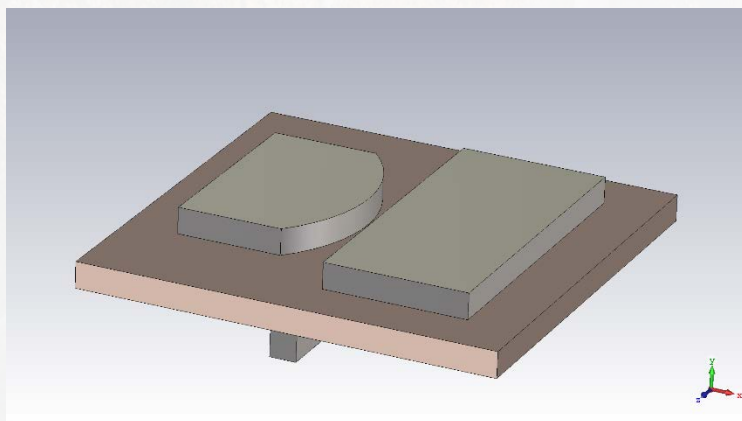




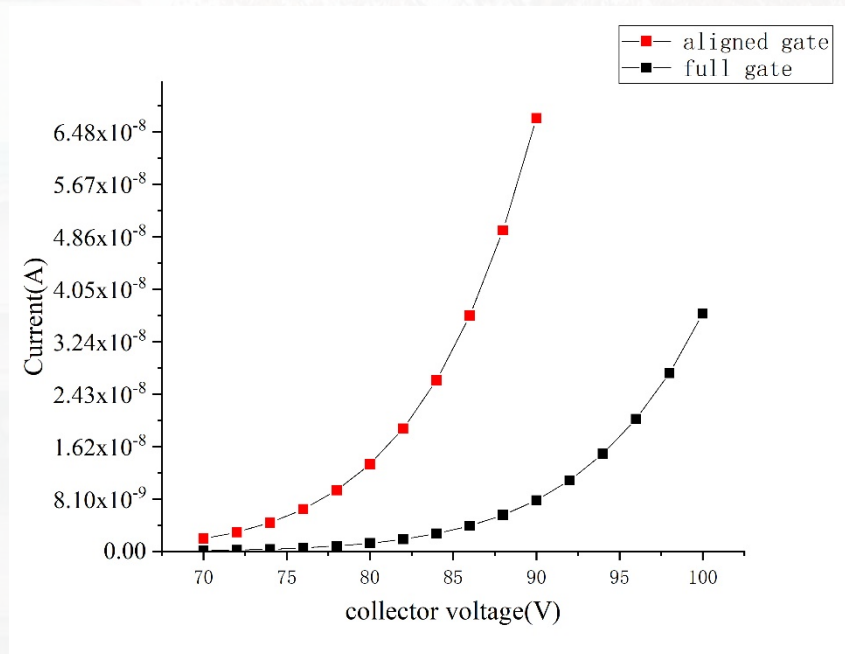
## Optimization: gate structure



Full back gate



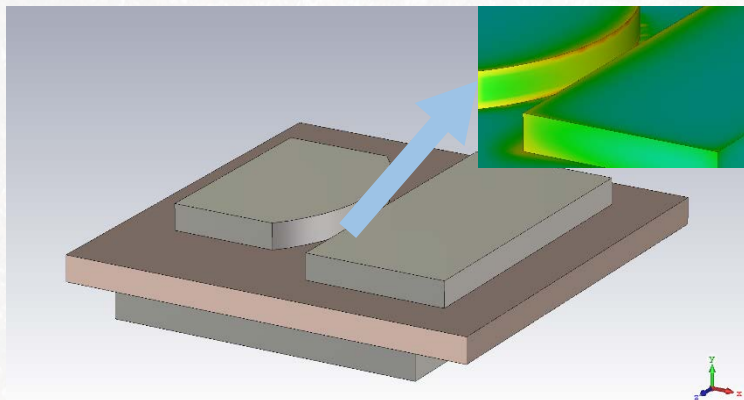
Aligned back gate



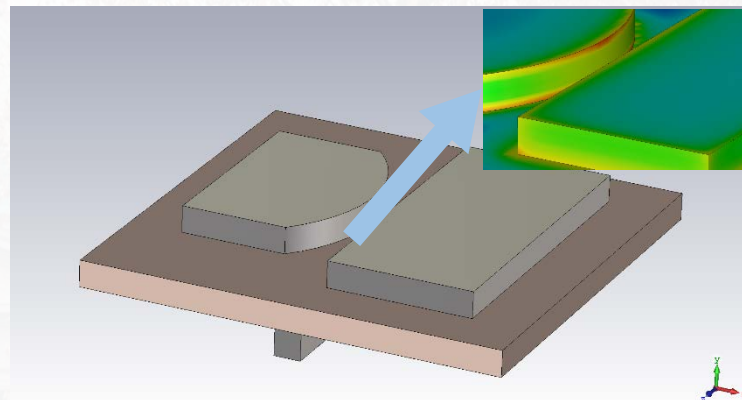
- Referring to the structure of MOSFET, aligned back gate is proposed
- Compared to full back gate, aligned back gate can obtain larger current and lower the threshold voltage



## Optimization: gate structure



Full back gate



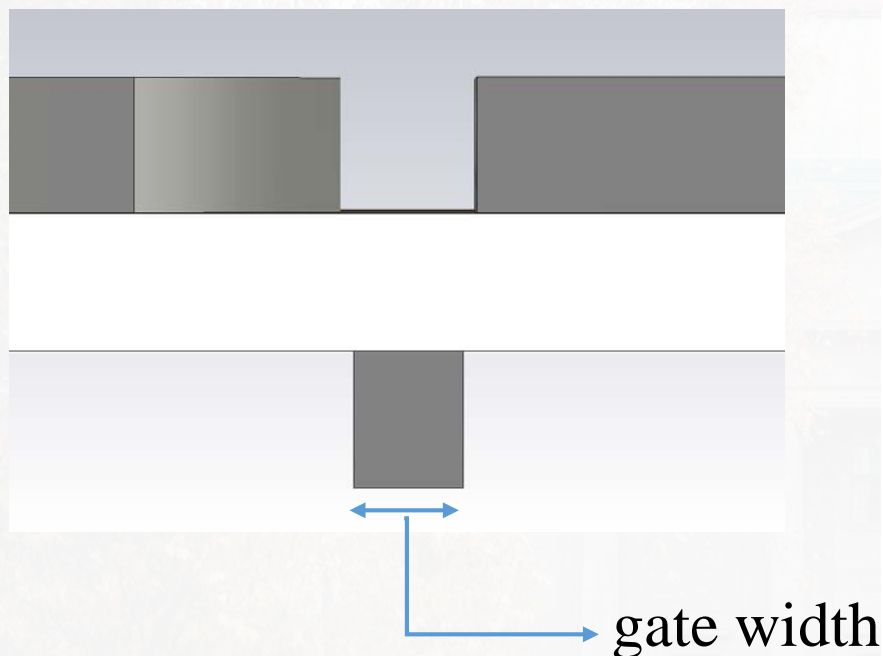
Aligned back gate

	Full back gate	Aligned back gate
Emission Current	7.9nA	67nA
Threshold voltage	92V	77V
Maximum electric field	$1.92 \times 10^9 \text{V/m}$	$2.3 \times 10^{10} \text{V/m}$



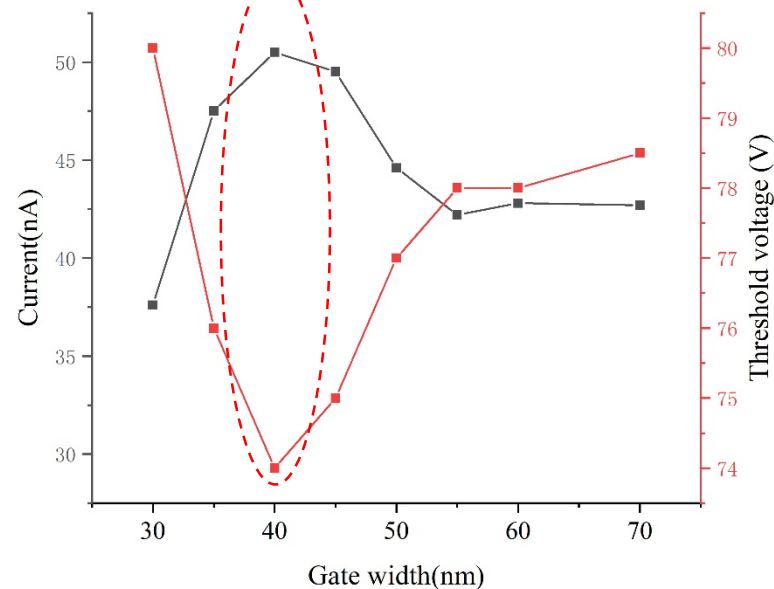


## Optimization: gate structure



Gap width: 50nm

A balance must be achieved between the operating current and the threshold voltage. Meanwhile, the accuracy of fabrication should also be considered



# CONTENT



**01** BACKGROUND

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**02** MAIN WORK

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**03** CONCLUSION

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**04** FUTURE WORK

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- Compared to flat structure, a “sharper” electrode can obtain a larger emission current, while a balance must be achieved between the turn-on voltage and the operating current
- Aligned back-gate structure can enhance the modulation ability of the device, increasing the electric field intensity by 11 times and the emission current by an order of magnitude

# CONTENT



**01** BACKGROUND

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**02** MAIN WORK

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**03** CONCLUSION

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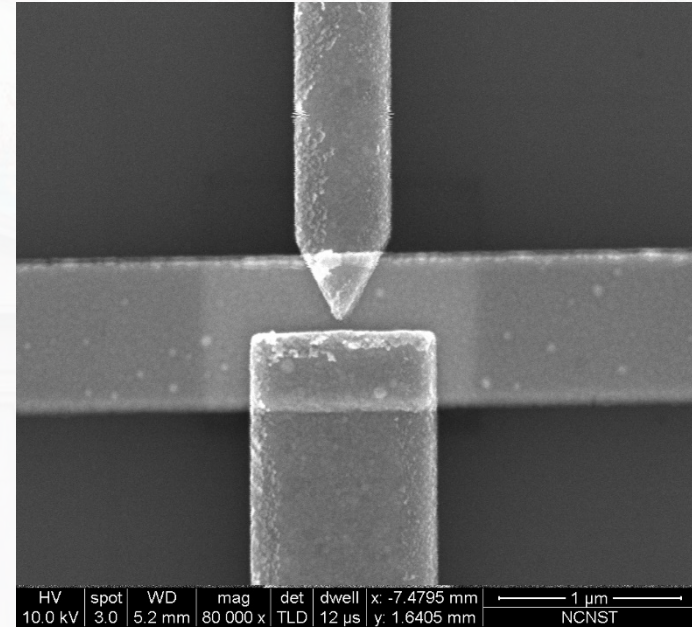
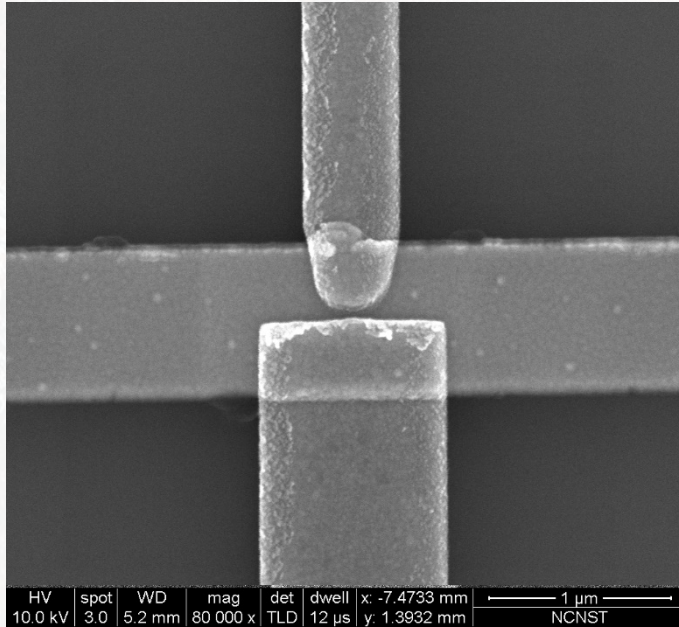
**04** FUTURE WORK

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## Future work



- Due to the accuracy of fabrication, the overlap area of the gate and the emitter should be improved in future work.
- Array structure can also be considered to achieve larger operating current.



# THE END

## Thanks for your listening !

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